#9/C

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2827

Amdt
4/E
J. McMillan
7/30/02

PATENT
Attorney Docket No. 401188/FUKAMI

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

MISUMI et al.

Application No. 09/848,256

Filed: May 4, 2001

Art Unit: 2827

Examiner: L. Thai

For: SEALED SEMICONDUCTOR DEVICE AND LEAD FRAME USED FOR THE SAME

RESPONSE TO OFFICE ACTION

Commissioner for Patents
Box AF
Washington, D.C. 20231

Dear Sir:

In response to the Office Action dated May 6, 2002, please enter the following amendments and consider the following remarks.

AMENDMENTS

IN THE CLAIMS:

Cancel claims 4-9, and 16 and replace the indicated claims with:

10. (Thrice Amended) A sealed semiconductor device comprising:

a semiconductor chip;

a lead frame including internal leads extending across part of and spaced from a surface of said semiconductor chip; and

a die pad separate from and not continuously connected to said lead frame and on which said semiconductor chip is mounted, wherein said lead frame includes protrusions extending substantially perpendicular to and contacting said die pad.

11. (Thrice Amended) A sealed semiconductor device comprising:

a semiconductor chip;

a lead frame including internal leads extending across part of and spaced from a surface of said semiconductor chip, and

a die pad separate from and not continuously connected to said lead frame and on which said semiconductor chip is mounted, said die pad including fixed protrusions extending toward and contacting some of said internal leads.

20. (Amended) The sealed semiconductor device according to claim 21, further comprising a die pad on which said semiconductor chip is mounted.

21. (Amended) A sealed semiconductor device comprising:

a semiconductor chip;

a lead frame including internal leads extending across part of and spaced from a surface of said semiconductor chip; and

a tape member located between said semiconductor chip and said internal leads to hold said semiconductor chip and said internal leads at a fixed distance from each other, said tape member having a first surface to which said internal leads are entirely bonded and fixed and a second surface, not fixed to but contacting the surface of said semiconductor chip.

22. (Amended) A lead frame and tape for a sealed semiconductor device having a rectangular semiconductor chip sealed within an encapsulating resin, the lead frame and tape comprising:

internal leads extending toward and electrically connected with wires to respective pads located approximately along a central axis of the semiconductor chip; and

a tape including four tape members, each tape member having a first surface to which some of said internal leads are fixed, each of said tape members being arranged at a respective corner of the semiconductor chip so that a portion of a second surface of each of said tape members contacts a surface of the semiconductor chip when the semiconductor chip is sealed within the encapsulating resin.

REMARKS

In response to the Official Action May 6, 2002, Applicants amend their application and request reconsideration. In this Amendment, claims 4-9 and 16 are cancelled leaving claims 10, 11, and 17-22 pending.

The errors in claims 16 and 21, generally typographical in nature, that led to the rejections of those claims as to form is regretted. However, the rejection is moot as to claim 16 in view of its cancellation and claim 21 is corrected.

Likewise, in view of the cancellation of claims 4-9 and 16 many of the prior art rejections are moot. Thus, only the rejections with respect to the remaining claims are discussed.

The invention concerns an encapsulated semiconductor chip and one that uses the so-called lead-on-chip (LOC) mounting arrangement. In that mounting arrangement, a complex lead frame including many internal leads is used to make electrical connections to electrodes on the semiconductor chip. As pointed out in the patent application, this structure permits the use of relatively large semiconductor chips. Electrode pads to which wire bonds are made are generally aligned along a centerline of the chip rather than being disposed along the peripheral edges of the chip, as in earlier technology.

An example of an LOC lead frame is illustrated in Figure 2 of the patent application. In LOC technology, a lead frame as shown in Figure 2 and as shown in every other figure in the patent application, is separate and distinct from a die pad, such as the die pad 3 shown in many figures of the patent application. The die pad supports the semiconductor chip, for example, the chip 1 in many of the illustrated embodiments. The chip is bonded to the die pad.

In many prior art lead frame structures, die pads are an integral part of a lead frame and are attached to the lead frame by so-called hanging leads that suspend the die pad from the other parts of the lead frame. The LOC structure does not employ a lead frame including an integral die pad because of the complexity and delicacy of the lead frame structure with the internal leads, for example, as shown in Figures 2 and 10 of the patent application.

Independent claims 10 and 11, which encompass the embodiments of Figures 22-27 and the corresponding descriptions, in the patent application, are amended to explain that the die pad is a distinct element, separate from and not continuous with the lead frame including the internal leads.

Claim 10 and its dependent claims 17 and 19 were rejected as anticipated by Tomita et al. (U.S. Patent 5,535,509, hereinafter Tomita).

In making the rejection, the Examiner placed emphasis upon Figures 21-25, 29, and 30 of Tomita. In those figures, an unusual lead frame structure is illustrated that includes an integral die pad. The die pad is adjusted to lie in a plane separate from and parallel to the plane

of the internal leads by the bending of a die pad support as is particularly illustrated in Figures 23, 25, 28, and 30 of Tomita. It is apparent that in the illustrated structures of Tomita, the support 111 is a continuous and integral part of the lead frame as well as of the die pad.

The sealed semiconductor device defined in claim 10 and its dependent claims includes a lead frame and a die pad but the lead frame and the die pad are separate elements, as shown in the embodiments of Figures 22-26, that are not continuous nor connected to each other as in Tomita. Rather, the die pad is separate and the lead frame includes protrusions that extend perpendicular to and contact the die pad. These protrusions help stabilize the structure so that during resin molding the die pad is not unduly displaced with respect to the lead frame and internal leads.

Clearly, Tomita cannot anticipate claim 10 or its dependent claims 17 and 19 because Tomita does not disclose all of the elements of claim 10 as presented here. Namely, there is no disclosure of an independent die pad and lead frame much less, in such an arrangement, protrusions extending from the lead frame substantially perpendicular to and contacting the die pad for stabilizing the die pad during resin encapsulation. Therefore, the rejection should be withdrawn.

Claim 11 was rejected as anticipated by Aoki (U.S. Patent 5,834,691). This rejection is respectfully traversed.

In the rejection, the Examiner placed reliance upon Figures 1-7 of Aoki. These figures of Aoki illustrate a conventional lead frame including an integrated die pad and internal leads. The die pad is suspended from part of the lead frame by the hanging leads 4 so that the die pad is continuously connected to the lead frame.

In claim 11 as presented here, just as in claim 10, the die pad and lead frame, i.e., internal leads, are independent elements that are not continuously connected. Aoki does not disclose such a structure and, for that reason, Aoki cannot anticipate claim 11.

Claim 18, a dependent claim depending from claim 10, was rejected as unpatentable over Tomita in view of Aoki. This rejection is respectfully traversed. It is readily apparent that neither Tomita nor Aoki describes the independent arrangement of a die pad and lead frame with internal leads as in the invention. Therefore, no combination of Tomita and Aoki could either disclose or suggest such a structure. Thus, the rejection of claim 18 cannot be properly maintained.

Examined claims 20-22 were rejected as anticipated by Lee, U.S. Patent 5,358,906. This rejection is respectfully traversed as to amended claims 20-22.

Amended claims 20-22 are fully supported by the patent application with respect to its Figures 1 and 2. Claim 20 has been amended to make it depend from claim 21. Amended claim 20 adds to the structure of claim 21 a die pad on which the semiconductor chip is mounted.

Claim 21 has been clarified because of the error pointed out by the Examiner. At the end of the claim, reference is now made, as originally intended, to the tape member rather than the semiconductor chip. In addition, language from claim 20 stating that the tape member is not fixed to but contacts the surface of the semiconductor chip is incorporated into claim 21. Thus, the limitations of amended claim 21, considering examined claim 20, present no new issues. Claim 22 is amended to describe the presence of four tape members constituting a tape. The four tape members are located at respective corners of a rectangular semiconductor chip that is employed with the claimed lead frame and tape. The presence of four such members is supported by Figure 2. There, the four tape members 8 are visible behind leads of the lead frame when that figure is carefully studied. Those members 8 are shown in cross-section in Figure 1.

With regard to claims 21 and 20, Lee discloses, in the cited figures, an insulating film 33 interposed between the leads 34b and the semiconductor chip 31. Whether that insulating film 33 is bonded to the leads and not bonded to the semiconductor chip cannot be determined from the disclosure of Lee. In other figures of Lee, a fluoroethylene film 53 is interposed between the semiconductor chip and the leads. The surface of this film is roughened to increase its "adhesion" to both the leads and the semiconductor chip. Whether there is any bonding between this film and either of the semiconductor chip and the leads is not apparent from Lee. What is apparent is that there is, desirably, adhesion between the film and both of the leads and the semiconductor chip, contrary to the structure described in claims 21 and 20.

With regard to claim 22, the most pertinent figure of Lee is Figure 8 which discloses the presence of two of the insulating films 53 between the leads and the semiconductor chip. Obviously, that disclosure cannot meet the limitations of amended claim 22 and therefore cannot anticipate that claim.

Reconsideration and a favorable Action on the remaining claims are earnestly solicited.

Respectfully submitted,

Jeffrey A. Wyand, Reg. No. 29,458
LEYDIG, VOIT & MAYER, LTD.
700 Thirteenth Street, N.W., Suite 300
Washington, DC 20005-3960
(202) 737-6770 (telephone)
(202) 737-6776 (facsimile)

Date: July 25, 2002

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2827

PATENT
Attorney Docket No. 401188/FUKAMI

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

MISUMI et al.

Application No. 09/848,256 Art Unit: 2827

Filed: May 4, 2001 Examiner: L. Thai

For: SEALED SEMICONDUCTOR DEVICE AND LEAD FRAME USED FOR THE SAME

AMENDMENTS TO SPECIFICATION, CLAIMS, AND ABSTRACT MADE IN RESPONSE TO OFFICE ACTION DATED MAY 6, 2002

Amendments to existing claims:

Cancel claims 4-9 and 16.

10. (Thrice Amended) A sealed semiconductor device comprising:

a semiconductor chip;

a lead frame including internal leads extending across part of and spaced from a surface of said semiconductor chip; and

a die pad separate from and not continuously connected to said lead frame and on which said semiconductor chip is mounted, wherein said lead frame includes protrusions extending substantially perpendicular to and contacting said die pad.

11. (Thrice Amended) A sealed semiconductor device comprising:

a semiconductor chip;

a lead frame including internal leads extending across part of and spaced from a surface of said semiconductor chip, and

a die pad separate from and not continuously connected to said lead frame and on which said semiconductor chip is mounted, said die pad including fixed protrusions extending toward and contacting some of said internal leads.

20. (Amended) ~~A~~ The sealed semiconductor device according to claim 21, further comprising~~:~~

~~a semiconductor chip;~~

a die pad on which said semiconductor chip is mounted~~;~~

~~a lead frame including internal leads extending across part of and spaced from a surface of said semiconductor chip; and~~

~~a tape member having a first surface to which said internal leads are entirely bonded and fixed, and a second surface not fixed to but contacting said semiconductor chip, to ensure a fixed distance between said semiconductor chip and said internal leads~~.

21. (Amended) A sealed semiconductor device comprising~~;~~:

a semiconductor chip;

a lead frame including internal leads extending across part of and spaced from a surface of said semiconductor chip; and

a tape member located between said semiconductor chip and said internal leads to hold said semiconductor chip and said internal leads at a fixed distance from each other, said tape member having a first surface to which said internal leads are entirely bonded and fixed and a second surface, ~~a part of the semiconductor chip~~ not fixed to but contacting the surface of said semiconductor chip.

22. (Amended) A lead frame and tape for a sealed semiconductor device having a rectangular semiconductor chip sealed within an encapsulating resin, the lead frame and tape comprising:

internal leads extending toward and electrically connected with wires to respective pads located approximately along a central axis of the semiconductor chip; and

a tape including four tape members, each tape member having a first surface to which some of said internal leads are fixed, each of said tape ~~member~~ members being arranged at a ~~position where~~ respective corner of the semiconductor chip so that a portion of a second surface of each of said tape ~~member~~ members contacts a surface of the semiconductor chip when the semiconductor chip is sealed within the encapsulating resin.